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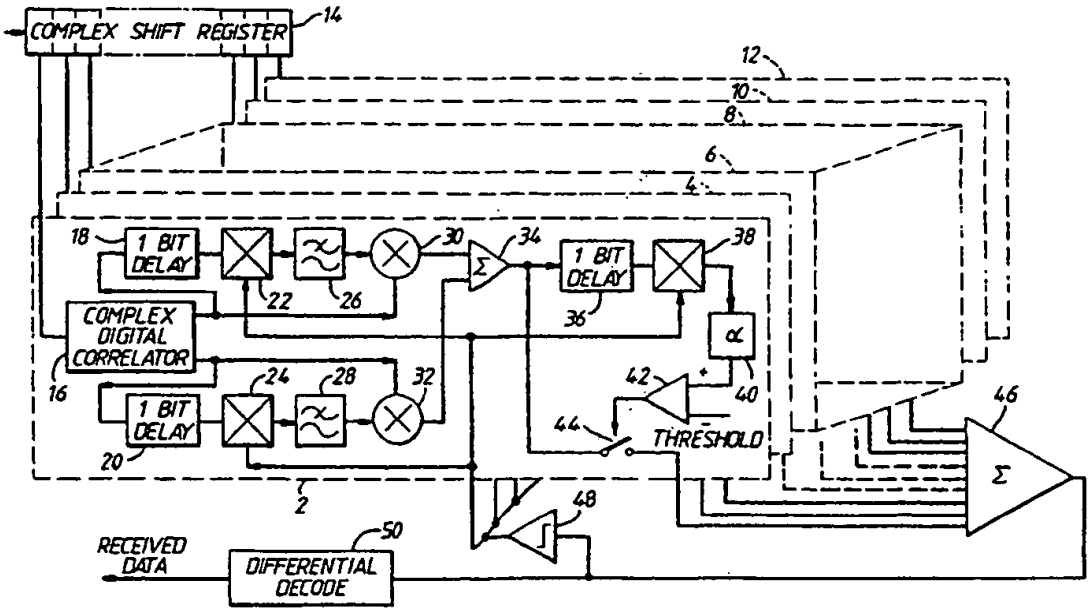
(54) Title: RAKE RECEIVER COMBINING ALL THE USEFUL MULTIPATH COMPONENTS OF A SPREAD SPECTRUM SIGNAL




(57) Abstract

Conventional Rake receivers for spread spectrum signals are typically restricted in the number of multipath components they can usefully combine. The present invention provides apparatus for combining all the useful multipath components in a received signal with modest complexity. Digital correlators are provided over the multipath delay spread of the signal at predetermined intervals and their outputs are maximal ratio combined. With close to rectangular transmission received filters, almost all the entire signal energy can be recovered at the output of the combiner even though no attempt is made to accurately align any of the correlators onto a specific multipath component.

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# RAKE Receiver Combining all the Useful Multipath Components of a Spread Spectrum Signal

The present invention relates to apparatus for use in equipment providing a digital radio link using direct sequence spread spectrum between a fixed and mobile radio unit.

Equipment for providing such a radio link is described in GB Patent Application Number 9304901.3. This application describes the use of Wiener-like filters for providing good estimates of the amplitude of the inphase I, the quadrature phase Q, components of, for example, a spread spectrum pilot signal.

Spread spectrum signals provide the possibility of obtaining excellent immunity to multipath fading through resolving the individual, time separated, multipath components and optimally combining them. The common approach for achieving this is to use a 'Rake' receiver as is familiar to those versed in the art. Such a receiver assigns de-spreading correlators to each of the dominant multipath components and synchronises them for maximum de-spread energy. For each of the Rake 'fingers' the phase and amplitude of the de-spread components is estimated and used to apply optimum amplitude weighting and phase alignment prior to addition (combining). The weighted sum of the multipath components will experience considerably less fading than any of the individual components so that a diversity gain is obtained.

One problem with the normal implementation of such a receiver is that the delay spread of the signal must be perpetually searched to determine whether a Rake finger should be assigned to a new, stronger, multipath component. If the channel is changing rapidly, significant loss in performance can result from there being too long a delay between a stronger multipath component appearing and it being assigned to a Rake finger.

Additionally some channels may consist of a large number of quite small multipath components. If all or most of these are not assigned to a Rake finger then a significant amount of signal energy may be wasted for the purposes of reception although it will still appear as interference to the reception of the spread spectrum transmission sharing the carrier frequency in a Code Division Multiple Access (CDMA) sense. The problem with these low level components is that, unless they are being measured continuously, it is not possible to assess with adequate accuracy, when and at what level they should be included in the combining output. The requirement to allow inclusion of a large number of multipath components could lead to the need for permanent provision of hardware for a large number of Rake fingers and a very fast searcher to assign the Rake fingers efficiently and rapidly.

Conventionally, every Rake finger would require a spread spectrum decorrelator, nominally timed aligned to the multipath component. Two identical spread spectrum decorrelators, assigned in time symmetrically either side of the first correlator

would be required. The time offset of these correlators will be typically plus or minus one quarter or one eighth of a chip interval. The chip interval is the spread bit period, ie. $\frac{\text{bit period}}{\text{spreading factor}}$. The sampling of the signal at four or eight times the chip rate becomes essential. These correlators together with the first form of code lock loop in which the energy on the three correlator outputs are compared and the timing of the code generators for the correlators are adjusted so that the energy on the centre correlator is always maximised, as familiar to those versed in the art. A phase estimator (typically a phase lock loop) to obtain the carrier phase of the signal for the purposes of phase compensation prior to combining, and, an amplitude estimator to apply optimum weighting to the signals prior to combining would also be required. The major complexity in terms of operations is in the three spectrum decorrelators.

The searcher would typically consist of a number of sliding correlators arranged together to cover the overall delay spread of the signal, perhaps sliding their timing in steps of half chips. If optimal performance in assigning Rake fingers to very weak multipath components is to be achieved then ideally the searcher would examine all multipath components in parallel. This would require a digital matched filter with a delay coverage equal to the maximum anticipated delay spread for the signal.

An object of the present invention is to provide means for combining the functions of the searcher and the Rake fingers

whilst reducing the sample rate to one sample per chip and greatly reducing the hardware complexity.

According to the present invention there is provided apparatus for use in equipment providing a digital radio link using direct sequence spread spectrum between a fixed and mobile radio unit, said apparatus comprising a Rake receiver including a plurality of digital correlators each providing a Rake finger, in which a block of digital correlation functions cover a contiguous span of spreading code phases of the same order as the maximum delay spread of a signal to be received, and adder means arranged to combine energy from each multipath component from several correlators.

Various embodiments of the present invention will now be described with reference to the accompanying drawings, in which;

FIGURE 1 shows a graph of non-optimal sampling of a correlation function,

FIGURE 2 shows a block diagram of a parallel Rake DBPSK receiver,

FIGURE 3 shows a block diagram of a serial Rake DPSK receiver,

FIGURE 4 shows a block diagram of a serial Rake BPSK receiver with a pilot signal,

FIGURE 5 shows a serial Rake MDPSK receiver,

FIGURE 6 shows a serial Rake MDPSK receiver having alternative energy measurement, and

FIGURE 7 shows a block diagram of a serial Rake MPSK receiver.

Firstly, consider a bank of digital correlators i=0 to n-1, each fed with a code shifted by one chip interval from the previous one. The total cover delay span is equal to N chips where N is chosen to give a delay span at least equal to the largest signal delay spread likely to be encountered in practice. Let it be assumed that the code has been synchronised such that the correlations performed on the end digital correlators de-spread all of the significant multipath components over the delay spread of the signal, ie. the delay coverage of the correlator bank is centred on the delay spread of the signal.

Each digital correlator serves to measure the signal power received at its timed position and also serves as a Rake finger for reception of that signal component whenever it is required to be combined. It will be appreciated that when using only one sample per chip it is not possible to align any digital correlator (or Rake finger) exactly, or even closely, onto a particular multipath component. This might seem to imply that significant losses in signal energy must arise. However, provided the transmission received filters of the spread spectrum link are suitably designed, this need not be the case.

If the transmission receive filters, which may be of Nyquist type, have been designed as linear phase with a very sharp (near to rectangular frequency in response) then very little energy will be aliased through sampling even at as low a rate as one sample

per chip. This raises the question as to how the energy is to be recovered. Let the position be considered where the multipath component is timed to arrive exactly half way between the optimum correlation times of a pair of adjacent correlators (this represents the worst case). Because of the auto correlation function of the received signal, imposed on the multipath component by the combination of the transmission received filter functions, both correlators will output some energy (in this particular case equal energy) corresponding to the multipath components arriving half way between them. Similarly, the further out correlators either side of the multipath component will output smaller energy levels. This effect is shown in Figure 1. In Figure 1 the curves shows the correlation function for a signal passed through an ideal rectangular filter. The arrows represent the timings of the correlators with significant energy. If the signal components from all correlator outputs (extending an arbitrary long time in both directions) were optimally combined then all of the signal energy corresponding to the multipath component could be recovered in spite of the incorrect sample timing. In practice, none of the ideals are satisfied. Thus the filter is not an ideal rectangular filter; combining is never optimum and only a few correlator outputs can usefully be combined. Nevertheless, experiments have shown that for practical filters, realistic combining and using the optimum (small) number of correlator outputs, the average loss due to non-optimum combining is typically less than 1 dB even for a very large number of multipath

components. This is partly because the performance is determined by an average of overall conditions and it is very unlikely that all multipath components will appear at exactly the worst sample points simultaneously.

Thus, by having a continuous bank of Rake fingers, the requirement for achieving optimum sample timing is removed. This has the following advantages. As mentioned above, sampling can take place at one sample per chip. This may permit significant cost/power consumption reductions on the analogue/digital convertors and initial digital signal processing operations. Each Rake finger now requires only one correlator. Code lock loop circuitry is not required for the individual Rake fingers. Since only one Rake correlator is required per chip offset, a modest number of correlators can cover the delay spread of the signal. Since the Rake correlators cover the entire delay spread of the signal they can also serve as the searcher. Essentially hardware/software associated with each Rake correlator independently decides whether the correlator output should be included in the combiner sum.

Referring to Figure 2, a parallel Rake differential binary phase shift keying (DBPSK) receiver is shown in block diagram form.

In Figure 2 there is shown a plurality of parallel Rake fingers 2, 4, 6, 8, 10 and 12. It will be appreciated that each Rake finger includes the circuit elements which will be described hereinafter with reference to Rake finger 2.

A complex shift register 14 receives the incoming data and has each stage connected to an input of a respective one of the complex digital correlators 16 in each Rake finger. The complex digital correlator 16 has two outputs, each is connected to an input of a one bit delay device 18, 20 and is further connected to an input of a linear multiplier 30, 32. An output of the one bit delay device 18 is connected to an input of a half linear multiplier 22 which has an output connected to an input of a Wiener-like filter 26. The output of the filter 26 is connected to a further input of the linear multiplier 30. Similarly, the output of the one bit delay device 20 is connected to an input of a half linear multiplier 24, the output of which is connected to the input of a Wiener-like filter 28. The output of the Wiener-like filter 28 is connected to a further input of the linear multiplier 32. The outputs from the linear multipliers 30, 32 are connected to a respective input of an adder circuit 34, the output of which is connected to an input of a one bit delay circuit 36. The output of the one bit delay circuit 36 is connected to an input of a further half linear multiplier 38, the output of which is connected to an input of an alpha tracker circuit 40. The alpha tracker circuit is the digital equivalent of an RC low pass filter. It is an integrator with leakage where the output, $S_n = \alpha.I_n + (1 - \alpha) S_n - 1$ ($I_n$ is the nth input sample). The output of the alpha tracker circuit 40 is connected to an input of a threshold circuit 42. Each Rake finger has an output line connected to an adder circuit 46. This output line has the output of the adder circuit 34 connected to it by a switching arrangement 44 which is

operated under the control of the threshold circuit 42. The output of the adder circuit 46 is connected to input of a limiting circuit 48 and to the input of a differential decode circuit 50. The limiting circuit 48 generates an output which is fed to a second input of the half linear multipliers 22, 24 and 38. The differential decode circuit 50 generates at an output the received data signal.

The operation of the circuit shown in Figure 2 will now be described.

The receiver shown in the Figure 2 is specifically for a differential binary phase shift keying (DBPSK) receiver. Each Rake finger 2-12 is subjected to a successive one chip delayed version of the signal as that signal is passed through the complex shift register 14. The complex digital correlator 16 is used to de-spread the I and Q components of that part of the signal arriving at the relevant time. The I component of the signal is passed to the one bit delay circuit 18 and the Q component is passed to the one bit delay circuit 20. The I and Q components are then passed through respective half linear multipliers 22, 24 which remove the modulation corresponding to the previous bit from the components. The I and Q components are then fed to the Wiener-like filters 26, 28. These filters give good estimates of the I and Q values corresponding to the received signal element at the time one bit earlier than the input. This prediction compensates for the input delay circuit. Multiplication of the I and Q components of the signal with the corresponding I and Q estimates of the unmodulated signal is carried out in the respective linear

multipliers 30, 32 and the outputs of these multipliers are summed in the summation circuit 34 to give a phase corrected and amplitude weighted version of the signal available for combining.

At this point in time it is not clear whether this output should be applied to the adder circuit 46 since it may consist only of noise. If the estimating Wiener-like filters were perfect they would indicate that the true signal components I and Q were in fact zero and the previous multiplication would have produced a zero output. However, the estimator outputs are never perfect and will always output some noise even when there is no signal component. Thus a second stage is required to determine whether a signal component adequate to justify inclusion is in fact present. The signal for potential inclusion is taken and delayed by a one bit period by the delay circuit 36 and the data for the previous bit is again stripped off by the linear multipliers 30, 32. The output at this stage is now a noisy measure of the energy in the correlator output in the previous bit interval. This is fed to an averaging filter 40. In this example the averaging filter is an alpha tracker. The output of the filter 40 is then compared with a threshold by threshold circuit 42 to determine when the signal component should be included in the overall combiner. The adder circuit 46 produces an overall output which is hard limited to produce the modulation for stripping off in the next demodulation frame. This is accomplished by the limiting circuit 48 which receives the output of the adder circuit 46 and the output of the hard limiter is connected to the half linear multipliers 22, 24, 38. When the

signal first appeared at the output of the limiting circuit 48 it will be random. Depending upon the number of Rake fingers and the overall characteristics of the signal, the receiver may be able to boot strap itself from this condition. Alternatively, each long transmission (consisting of several transmission frames) can be prefaced with a period of transmitting known data. During this period the locally known data is used to derive the modulation for stripping and the stripping input is switched over to the Rake output limiting circuit only when the known data is replaced with unknown data.

The output of the adder circuit 46 is differentially decoded in the conventional fashion by multiplying each sample output by the previous one. This process is carried by the differential decode circuit 50.

If the multiplier is linear on both inputs, ie. several bits precision, then the amplitude of the output is a suitable soft decision metric for use in conjunction with soft decision error correction decoding if error control coding has been applied to the transmit data.

As an alternative to the above described implementation, an alternative implementation will now be described with reference to Figure 3 which shows a serial Rake differential phase shift keying (DPSK) receiver.

With reference to Figure 3, the complex digital match filter 52 receives the inphase and quadrature phase signals on the respective lines I, Q. The filter 52 has two output lines one of

which is connected to an input of a one bit delay device 56 and the other is connected to an input of a one bit delay device 58. The output of the one bit delay device 56 is connected to an input of a half linear multiplier 60 the output of which is connected to an input of a Wiener-like filter 64. The output of the Wiener-like filter 64 is connected to an input of a linear multiplier 68, the output of which is connected to an input of an adder circuit 72. The output of the one bit delay device 58 is connected to an input of a further half linear multiplier 62, the output of which is connected to an input of a Wiener-like filter 66. The output of the Wiener-like filter 66 is connected to an input of a linear multiplier 70, the output of which is connected to a further input of the adder circuit 72. The output of the adder circuit 72 is connected to an input of a further one bit delay circuit 74 and to an input of switching arrangement 84. An output of the one bit delay device 74 is connected to a further half linear multiplier 76, the output of which is connected to an alpha tracker circuit 78. An output of the alpha tracker circuit 78 is connected to an input of a threshold device 80, the output of which is used to control the switching arrangement 84. The switching arrangement 84 is connected to the input of an integrating circuit 82. An output of the integrating circuit 82 is connected to an input of a limiting device 86 and to the input of a differential decode circuit 88. The differential decode circuit 88 generates the received data. An output of the limiting device 86 is connected to a further input of the half linear multipliers 60, 62, 76.

A memory 54 is connected to a further input of the one bit delay devices 56, 58 and 74, and is also connected to a further input of the Wiener-like filters 64 and 66, and to a further input of the alpha tracker circuit 78.

The operation of the circuit shown in Figure 3 will now be described.

The circuit produces an output for each chip time interval within the delay window for each chip. The basic operation is identical to that of Figure 2 except that as each new output is produced for each successive chip offset it may, depending on the average signal strength received for that offset be fed to an accumulator, shown as an integrator 82. The I components of the signal are passed via the one bit delay circuit 56, the half linear multiplier 60, the Wiener-like filter 64, the linear multiplier 68 and the adder circuit 72. The Q components of the signal are passed via the one bit delay circuit 58, the half linear multiplier 62, the Wiener-like filter 66, the linear multiplier 70 and the adder circuit 72. When the end of the span for receipt of the current bit is reached the output of the adder circuit 72 is hard clipped for the purposes of stripping the data and differentially is decoded to provide the overall receiver output. The control of the output of the adder circuit 72 is achieved by the switching arrangement 84 which is controlled by the threshold circuit 80, the alpha tracker 78, the further half linear multiplier 76 and one bit delay device 74 as described with reference to Figure 2. The output of the integrating circuit 82 is applied to the hard limiting

device 86 the output of which is fed back to the further inputs of the half linear multipliers 60, 62, 76. The output of the integrating circuit 82 is also passed to the differential decode circuit 88 to generate the received output data.

The memory 54 is needed in this embodiment because the contents of each of the Wiener-like filters and the alpha tracker circuit, as well as the one bit delay devices must be reinstated with the contents which they had when de-spreading the corresponding chip one bit earlier. The inclusion of the memory 54 enables the Wiener-like filters and the alpha tracker circuit to behave as though many more have been provided.

Referring to Figure 4, a binary phase shift keying (BPSK) receiver will now be described suitable for use with a pilot signal. Figure 4 represents a serial approach to such a receiver and includes a complex digital matched filter 90 for the pilot signal, and a complex digital matched filter 92 for the data signal. The I and Q components of the input signal are each applied to respective inputs of the filters 90, 92. The filter 90 has two outputs each connected to a respective Wiener-like filter 94, 96. The outputs of the Wiener-like filters are connected to an input of linear multipliers 102 and 104 respectively and also to first and second inputs of further linear multipliers 108, 110 respectively. An output from each of the linear multipliers 102, 104 are applied to a respective input of an adder circuit 106, the output of which is connected to one side of the switching arrangement 118. Another side of the switching arrangement 118 is connected to an

input of an integrating circuit 120 the output of which generates the received data signals.

An output of the multipliers 108, 110 are each connected to a respective input of a further adder circuit 112, the output of which is connected to an input of an alpha tracker circuit 114. The output of the alpha tracker circuit 114 is connected to an input of the threshold circuit 116, the output of which controls the switching arrangement 118. A memory 112 is connected to the Wiener-like filters 94, 96, the delay circuits 98, 100 and to the alpha tracker circuit 114 to reinstate their contents which they had when de-spreading the corresponding chip one bit earlier.

The operation of the receiver shown in Figure 4 will now be described. It will appreciated that while the description is applicable to a serial receiver a BPSK receiver could be embodied in parallel form.

Separate correlators are required for de-spreading the I and Q components of both the pilot and the signal for each one chip interval over the delay spread of the signal. Correlators will be essentially the same but will use different chip sequences. On the pilot output path the I and Q components are applied to the Wiener-like filters 94, 96 respectively, which have a symmetrical structure and a delay. This provides more reliable estimates of the carrier components at the particular delay being de-spread by averaging over a longer period and by avoiding the need to predict. Note that since the pilot is unmodulated, there is no need to strip off the data. The estimates of the carrier I and Q

components for the relevant point in the delay spread are used to compensate the phase and amplitude of a suitably delayed de-spread signal. The contents of the filters need to be reinstated from the memory 122 for each chip position within a bit, so here for the case of a BPSK receiver the same requirement applies. The outputs of the Wiener-like filters 94, 96 and the outputs from the delay circuits 98, 100 are, for the I and Q components respectively, combined by the linear multipliers 102, 104. The output signals from the linear multipliers 102, 104 are applied to an adder circuit 106 the output of which is connected by the switching arrangement 118 to the integrating circuit 120. The control of the switching arrangement 118 is governed by a threshold circuit 116 which receives an output signal from the alpha tracker circuit 114. The input to the alpha tracker circuit is derived by the adder circuit 112 which receives the output signals from two further linear multipliers 108, 110 which receives at both their respective inputs the output from the Wiener-like filters 94, 96 respectively.

As mentioned above, the output from the adder circuit 106 is fed via the switching arrangement 118 to the integrating circuit 120 under the control of the threshold circuit 116 which generates a conditional on average signal level. The integrating circuit 120 serves to perform the combining across the Rake components.

The signal measurement for the thresholding is obtained from the pilot by the further pair of multiplying circuits 108, 110. This is because the pilot signal will generally be stronger than the

data signal so can give a more accurate (noise free) estimate of the signal level. The embodiment described with reference to Figure 4 does not require the stripping of data because the pilot signal is available without any data thus the effects of any decision errors can be avoided.

In cases where the data signal is stronger than the pilot signal, this might apply for high data rate transmissions, it might be advantageous to perform the signal measurement on the basis of the data signal in the same manner as described with reference to Figure 3.

With reference to Figure 5, a multi phase differential phase shift keying receiver will now be described.

A complex digital matched filter 124 receives the inphase, I signal, and the quadrature phase, Q signal. The filter 124 has two output lines each being connected to the first input of a respective linear multiplier 136, 138. The output lines of the filter 124 are also connected to an input of a one bit delay circuit 126, 128 respectively. The outputs of the one bit delay circuits are connected to an input of a complex linear multiplying circuit 130 respectively which has two output lines connected to an input of a Wiener-like filter 132, 134 respectively. The output from each of the Wiener-like filters 132, 134 are connected to a second input of the linear multipliers 136, 138 respectively. The output from the linear multipliers 136, 138 are connected to an input of a further one bit delay circuit 140, 142 respectively, the outputs of which are connected to an input of a further complex linear multiplying

circuit 144 respectively. The complex linear multiplying circuit 144 has two output lines connected to an input of an adder circuit 146, the output of which is connected to an alpha tracker circuit 148. The one bit delay circuits 126, 128, 140, 142, the Wiener-like filters 132, 134 and the alpha tracker circuit 148 each have an additional input connected to a memory 174 for refreshing purposes. An output from the alpha tracker circuit 148 is connected to an input of a threshold detector circuit 149 the output of which is connected in a manner to control two switching arrangements 164, 166. The switching arrangements 164, 166 are connected to an output of the linear multiplying circuit 136, 138 respectively, and are used to apply that output to an input of a integrating circuit 160, 162 respectively. An output from each integrating circuit is applied to a differential decode circuit 172 which generates the data output signal. The outputs from the integrating circuits 160, 162 are connected to an input of a normalised amplitude and threshold to nearest phase in alphabet circuit 170 respectively. This circuit has two output lines connected to an input of a complex conjugate circuit 168 respectively, which has two output lines each being connected to a further input of the complex linear multiplying circuits 130, 144 respectively.

The operation of the receiver shown in Figure 5 will now be described.

The basic operation is the same as for the DBSPK receiver except that now the stripping for the pilot extraction must be

performed by a complex linear multiplier 130. Moreover, after phase and amplitude compensation, there is signal energy on both the I and Q components so Rake combining must be performed separately for both. For this purpose two separate integrating circuits 160, 162 are provided which perform combining across the different multipath components for both the I and Q signals. Measurement of the signal energy for the purpose of thresholding now requires removal of the data from the phase compensated signal, and this is achieved by using a further complex linear multiplier 144 with the data estimate. The two switching arrangements 164, 166 are used to control the input of the integrating circuits 160, 162. For data stripping the output of the integrating circuits 160, 162 is normalised to give a complex number containing only phase information. This operation is carried out by the circuit 170. After normalisation the phase is rounded to the nearest phase in the modulation alphabet, again by circuit 170. Data stripping requires complex multiplications with the complex conjugate of this data, so the output from the circuit 170 is applied to the complex conjugate circuit 168. Since differential modulation is used the user data must be obtained by a differential decoder 172. The current output of the integrating circuits 160, 162 is referred to as the complex number $Z_n$ and the previous output, $Z_{n-1}$ and the data differentially encoded between the nth and the n - 1th signalling intervals can be obtained by selecting the phase in the modulation alphabet nearest to the phase of $Z_n.Z^*_{n-1}$.

The signal measurement for purposes of thresholding may more conveniently be described using the architecture shown in Figure 6.

Figure 6 is similar to Figure 5 and like components have been given like designations and their function are as described with reference to Figure 5.

It will be noted that the difference between the two figures is the removal of the one bit delay circuits 140, 142 and the second complex linear multiplier circuit 144. This circuitry has been replaced by two further linear multipliers 178, 176 which receive the output from the Wiener-like filters 132, 134 at their two inputs, respectively. The outputs of the further linear multiplying circuits 178, 176 are connected to the adder circuit 146.

The energy measurement is performed by squaring the estimates on the I and Q signal channels directly. Because of the averaging involved in the Wiener-like filtering it is no longer necessary to perform the second multiplication as frequently as once per bit.

For a general case of multiple phase shift keying (MPSK) having a pilot signal the possible architecture is shown in Figure 7.

Figure 7 shows a comprehensive Rake MPSK receiver. The receiver includes a first complex digital matched filter 180 for the pilot signal and a second complex digital matched filter 182 for the data signal. The inphase I, and quadrature phase Q, components of the input signal are applied to both filters. The

pilot filter 180 has two output lines each connected to a Wiener-like filter 184, 186 respectively. The data signal filter 182 has two output lines each connected an input of a respective delay circuit 188, 190. An output from the Wiener-like filter 184 and an output from the delay circuit 188 is connected to an input of a linear multiplier 192 respectively. The output from the Wiener-like filter 186 and from the delay circuit 190 is connected to an input of a linear multiplier 194 respectively. Two further linear multipliers 196, 198 each receive at their inputs the output from a respective one of the Wiener-like filters 184, 186. The outputs from the linear multipliers 192, 194 are connected to an input of a switching arrangement 210, 212 respectively. The output from the further linear multipliers 196, 198 are applied to an input of an adder circuit 200 respectively. The output of the adder circuit 200 is connected to an input of an alpha tracker circuit 202 the output of which is applied to an input of a threshold detecting circuit 204. The output from the threshold detecting circuit 204 is used to control the switching arrangements 210, 212. Two integrating circuits 206, 208 have their input connected to a further input of a switching arrangement 210, 212 respectively, and the outputs from the integrating circuits are applied to a circuit 214 which selects the closest phase in the alphabet to generate the data output.

The only difference between the multi level PSK receiver and the BPSK receiver is that the inphase I and quadrature phase Q components must be handled separately in the combiners and

the demodulation is performed by selecting the phase in the modulation alphabet which is closest to the phase of the received signal. If the received signal had been forward error correction encoded in the transmit source then the complex signal at the output of the two integrating circuits 206, 208 would be used directly, providing self decision information.

The above receivers as described with reference to Figures 2 to 7 assume that the spreading code has already been synchronised to the extent that all of the significant multipath components fall within the span of the de-spreading functions related to the bank of correlators.

Initial synchronisation may be achieved in a number of ways. It is assumed that, for the pilotless case an unmodulation signal is transmitted during the initial synchronisation phase. Because the bank of correlators covers a wide delay spread in parallel, it may be used in a block search strategy in which a set of code phases is applied to the correlators and the measuring circuits examined for significant energy. If no significant energy is found in any of the energy measurement circuits, the set of code phases applied to the correlators is stepped forwards or backwards to cover the next contiguous (non-overlapping) range of delays and so on until either a signal is found or the entire uncertainty window is covered. In the latter case the set of code phases will be reset to the beginning or end of the uncertainty window. Alternatively the search strategy could run backwards from this point. When at least one correlator with significant

energy is found, the primary search strategy is stopped. At this stage part of the signal delay spread is covered by the code span of the bank of correlators. A secondary finding strategy is then required to perform the initial centring of the code span onto the delay spread of the signal. Once all the significant multipath components have been detected, the earliest and latest significant multipath components detected with the time spread window of the receiver are identified. At this stage it is possible that multipath components exist either side of the time spread window, but not both sides. The only way to be certain that the correct alignment is achieved is to test both hypotheses in turn as follows:

1) Shift the code phase so that the earliest path found moves close to the start of the coverage span. After a period of averaging, a new latest path will arise. The difference in times (correlator numbers) between the earliest and the last paths gives the captured delay spread for this case.

2) Shift the code phase so that the original latest path found moves close to the end of the coverage span. After a period of averaging, a new earliest path will arise. The difference in times between the earliest and last paths gives the captured delay spread for this case.

The code timing is finally aligned in the position of case 1 or case 2 according to which gave the greater captured delay spread.

The shifting of code phases can be achieved by the movement of pointers to locations in the memory. There is no

need physically to copy the contents of filters or delay circuits. In the parallel case it becomes necessary either to shift the contents of the various filters and delay circuits or, effectively, to rewire the connections between each Rake finger and the overall shift register.

Once initial synchronisation has been achieved it is necessary to maintain overall synchronisation to keep the code coverage of the receiver centred on the delay spread of the signal. This can be achieved as follows:

1) If the time spread window of the receiver is large enough so that it can be guaranteed that it will always exceed the signal delay spread by a significant margin then timing control can be exerted by regularly updating the code timings to keep the current earliest and latest found signal components centred on the time spread window.

2) If the above cannot be guaranteed it will be necessary to search outside the window with a separate sliding correlator. However, a simple single correlator should suffice for this case since the centring of the overall delay spread should change very slowly, being dependent only on overall changes in path length.

It will be readily appreciated by those skilled in the art that the receiver architectures described above can readily be extended to a dual pass receiver architecture such as that described in GB Patent Application Number 9309748.3.

## CLAIMS

1. Apparatus for use in equipment providing a digital radio link using direct sequence spread spectrum between a fixed and mobile radio unit, said apparatus comprising a Rake receiver including a plurality of digital correlators each providing a Rake finger, in which a block of digital correlation functions cover a contiguous span of spreading code phases of the same order as the maximum delay spread of a signal to be received, and adder means arranged to combine energy from each multipath component from several correlators.

2. Apparatus as claimed in Claim 1, wherein the Rake receiver includes receive and transmit filters of Nyquist type for creating a receive correlation function to permit recovery of mis-timed signal components in the correlator output signals.

3. Apparatus as claimed in Claim 2, wherein the Rake fingers are arranged in parallel and each Rake finger includes digital correlator means connected to a stage of a shift register means respectively, through which the input signal is passed, said digital correlator means having two output lines connected to a first input of first multiplying means and to a first input of second multiplying means via delay means, said second multiplying means having an output connected to a Wiener-like filter having an output connected to a second input of said first multiplying

means, said first multiplying means having their respective outputs connected to further adder means having an output connected to a switching arrangement, and an output connected to a third multiplying means via further delay means, an output from said third multiplying means being connected to an input of tracking means having an output connected to threshold means generating an output signal for controlling said switching arrangement, and, upon operation of said switching arrangement the output from said further adder means is applied to an input of said adder means which receives a signal from each of said Rake fingers, said adder means generating an output signal which is applied to an integrating means for generating a feedback control signal for each of the second multiplying means, said output from said adder circuit being also applied to a differential decode circuit for generating a received data output signal.

4. Apparatus as claimed in Claim 2 having only one Rake finger comprising a digital filter means arranged to receive the inphase and quadrature phase components of an input signal, said filter means having two output lines connected to a first input of first multiplying means and to an input of second multiplying means via a delay circuit, said second multiplying means having an output connected to an input of a Wiener-like filter, the output of which is connected to a second input of said first multiplying means, an output from each first multiplying means being applied to an input of adder means, the output of which is applied via

delay means to third multiplying means having an output connected to an input of tracking means, an output from said tracking means being applied to threshold means, an output of which is used to control a switching arrangement, said switching arrangement being connected to the output of said adder means and is arranged to switch said output to an integrating means, the output of which is connected to an input of a limiting means which generates an output which is applied to a further input of said second multiplying means, said output from said integrating means being further applied to a differential decode circuit which is arranged to generate the received data output signal.

5. Apparatus as claimed in Claims 3 and 4, wherein the Rake receiver is arranged to handle differential phase shift keying signals.

6. Apparatus as claimed in Claim 2, wherein digital filter means is provided respectively for a pilot signal and for the data signal, each being arranged to receive the inphase and quadrature phase components of an input signal, said filter for handling the pilot signal has its outputs connected to a Wiener-like filter, the outputs of which are connected to a first input of a first multiplying means and to first and second inputs of second multiplying means, said filter for handling the data signal has its output connected via delay means to a second input of said first multiplying means, an output from said first multiplying means being applied to an input

of first adder means respectively, said first adder means having an output connected to a switching arrangement, said second multiplying means having an output connected to an input of a second adder means respectively, an output of which is connected to an input of a tracking means, said tracking means being connected to threshold means arranged to control said switching arrangement, and upon operation of said switching arrangement the output from said first adder means is applied to an input of integrating means which generates at an output the received data signal.

7. Apparatus as claimed in Claim 6, being arranged to handle binary phase shift keying signals.

8. Apparatus as claimed in Claim 6 or Claim 7, wherein a plurality of Rake fingers may be arranged in parallel.

9. Apparatus as claimed in Claim 8, wherein the Rake receiver may comprise a serial and parallel combination of Rake fingers.

10. Apparatus as claimed in Claim 2 arranged to handle multi level differential phase shift keying signals, said apparatus comprising a digital filter means arranged to receive the inphase and quadrature phase components of an input signal, said filter having two output lines connected to a first input of multiplying means and to inputs of a first complex linear multiplying means

via delay means, said complex linear multiplying means having an output connected to a Wiener-like filter respectively, said filter having an output connected to a second input of said multiplying means, an output from said multiplying means being connected to an input of a further complex linear multiplying means via delay means and to a respective switching arrangement, said further complex linear multiplying means having its outputs connected to further adder means, an output of which is applied to an input of tracking means, an output from said tracking means is connected to a threshold device arranged to provide an output signal for controlling said switching arrangements, said switching arrangements being caused to operate to switch the output from said multiplying means to an input of an integrating means respectively, said integrating means having their outputs connected to a differential decode circuit which is arranged to generate a data output signal, said output from said integrating means being further applied to inputs of circuit means arranged to normalise amplitude and threshold to the nearest phase in alphabet and to generate output signals for processing by conjugate circuit means, said conjugate circuit means generating output signals which are applied to two further inputs respectively of said complex linear multiplying means and said further complex linear multiplying means.

11. Apparatus as claimed in Claim 10, wherein said further complex linear multiplying means and delay means associated

therewith is replaced by two further multiplying means each arranged to receive at its inputs the output from a Wiener-like filter respectively.

12. Apparatus as claimed in Claim 10, wherein a plurality of Rake fingers is arranged in parallel.

13. Apparatus as claimed in Claim 11, wherein a plurality of Rake fingers is arranged in parallel.

14. Apparatus as claimed in Claim 10 or Claim 11 comprising a serial/parallel combination of Rake fingers.

15. Apparatus as claimed in Claim 2, wherein a digital filter means is provided for a pilot signal and a further digital filter means is provided for the data signal, said filters being arranged to receive both the inphase and quadrature phase components of an input signal, said filter handling said pilot signal having two outputs each arranged to be connected to an input of a Wiener-like filter respectively, an output of which is connected to an input of a first multiplying means and to first and second inputs of a further multiplying means, said filter handling said data signal having two outputs arranged to be connected via delay means to a second input of said first multiplying means respectively, an output of said first multiplying means being connected to an input of a switching arrangement respectively, said further multiplying

means having an output connected to an input of further adder means respectively, the output of which is connected to tracking means, an output of said tracking means being applied to a threshold device which is arranged to generate an output signal for controlling said switching arrangements, said switching arrangements causing said output from said first multiplying means to be applied to an input of an integrating means respectively, said integrating means having an output connecting to circuit means which selects the closest phase in alphabet to generate a data output signal.

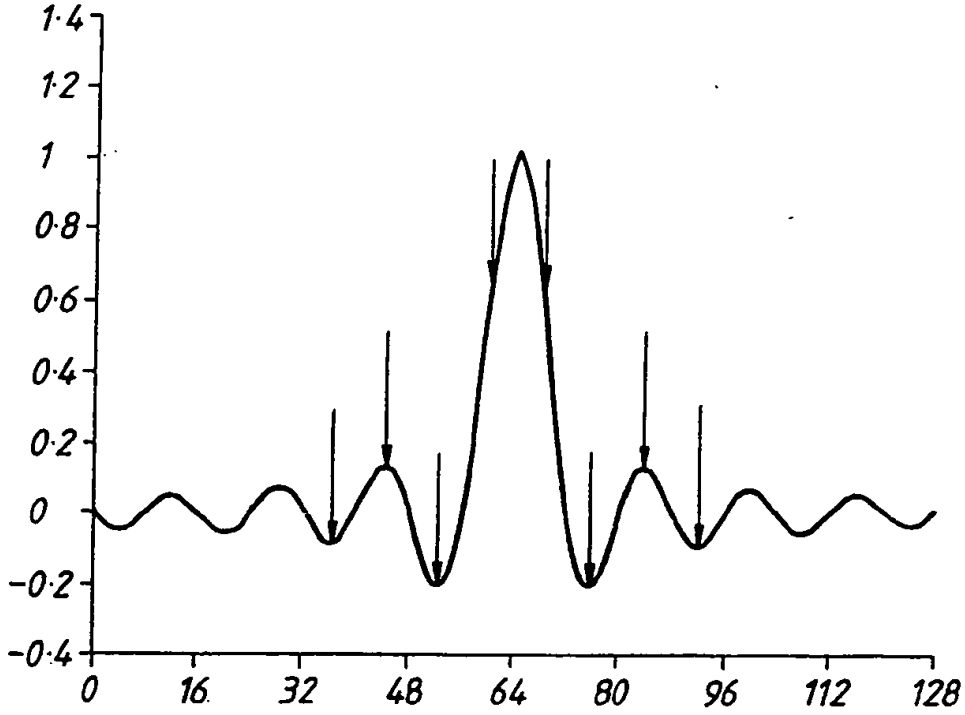
16. Apparatus as claimed in Claim 15 arranged to handle multi phase shift keying signals in serial, parallel or serial/parallel combination.

17. Apparatus as claimed in Claims 4, 6, 10, 11 and 15, wherein a memory means is connected to said delay means, Wiener-like filters and tracking means for refreshing their content with information relating to an earlier bit period.

18. Apparatus as claimed in any preceding claim, wherein to provide synchronisation said correlators have a set of code phases applied to them stepped forward or backward to cover the next contiguous range of delays, until either a signal is found the entire predetermined range is covered.

19. Apparatus as claimed in any of the preceding Claims 1 to 17, wherein synchronisation is provided by one or more sliding correlators arranged to scan outside the desired range.

20. Apparatus as claimed in any of the preceding Claims 3 to 19, wherein the Wiener-like filters are dual pass Wiener-like filters.


1·4
1·2
1
0·8
0·6
0·4
0·2
0
-0·2
-0·4
0
16
32
48
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80
96
112
128

Fig. 1

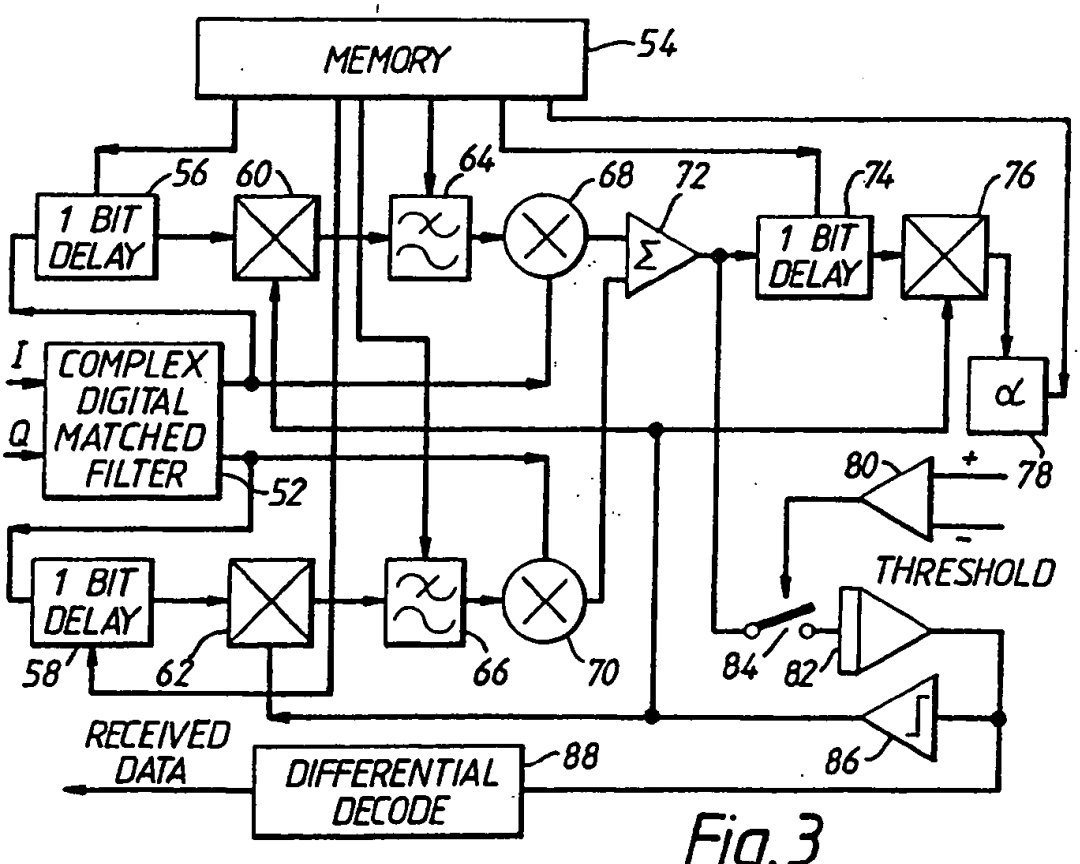
MEMORY
54
1 BIT DELAY
56
60
64
68
72
1 BIT DELAY
74
76
I
Q
COMPLEX DIGITAL MATCHED FILTER
52
α
78
80
+
-
THRESHOLD
1 BIT DELAY
58
62
66
70
84
82
RECEIVED DATA
DIFFERENTIAL DECODE
88
86

Fig. 3

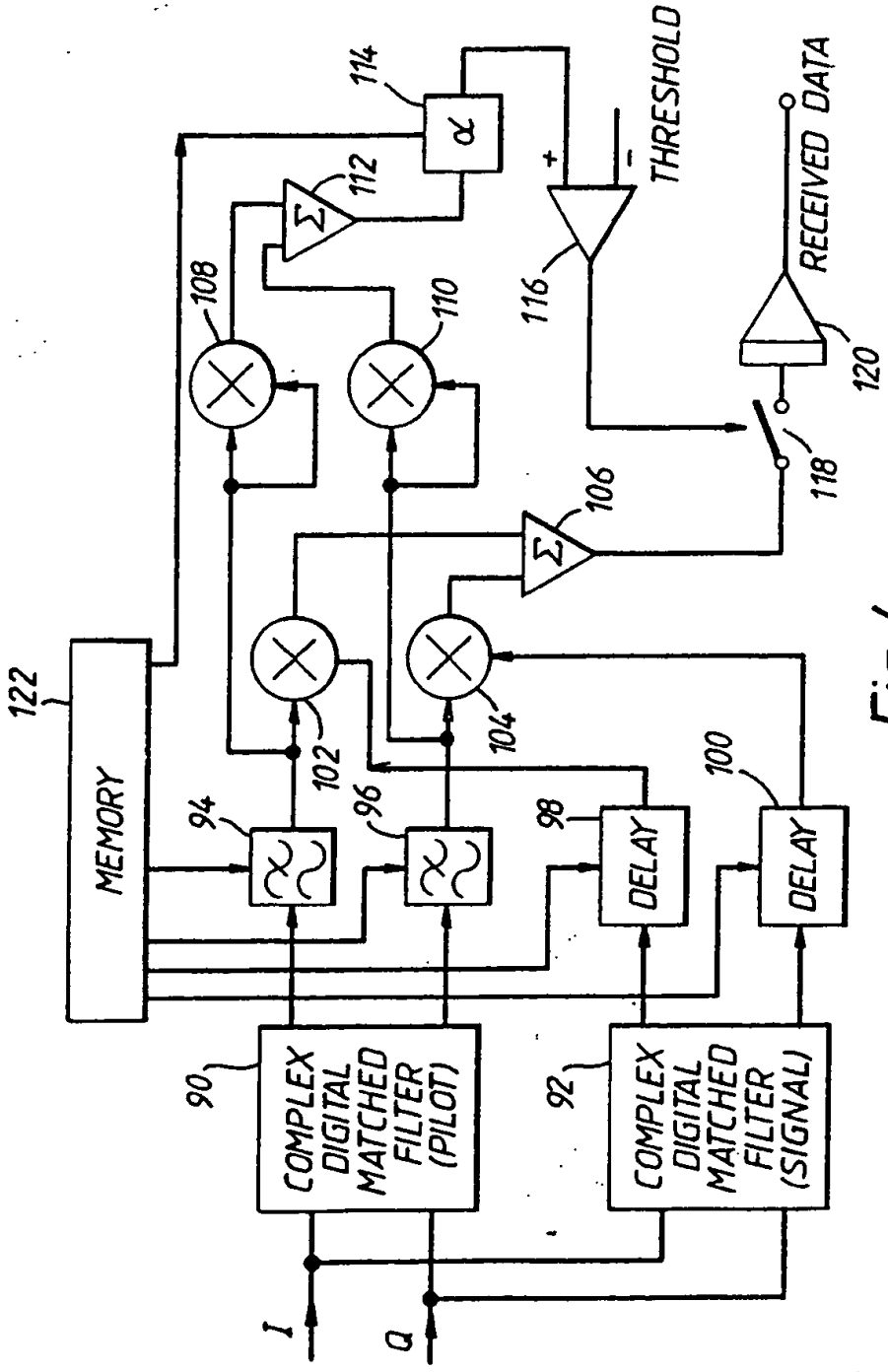
COMPLEX DIGITAL MATCHED FILTER (PILOT)
COMPLEX DIGITAL MATCHED FILTER (SIGNAL)
DELAY
DELAY
MEMORY
THRESHOLD
RECEIVED DATA
I
Q
90
92
94
96
98
100
102
104
106
108
110
112
114
116
118
120
122
Σ
Σ
α

Fig. 4

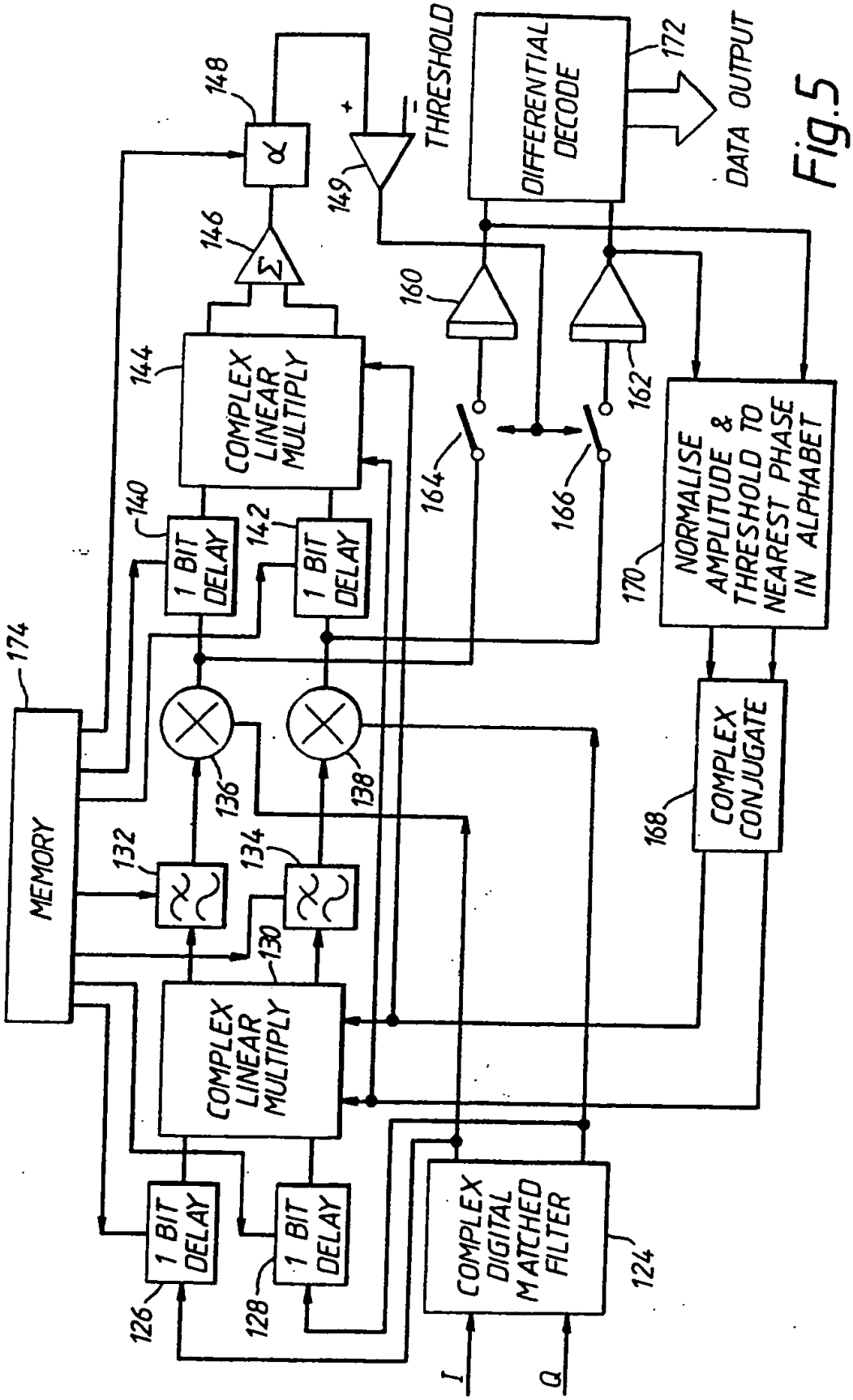
MEMORY
174
COMPLEX LINEAR MULTIPLY
130
COMPLEX LINEAR MULTIPLY
144
1 BIT DELAY
126
1 BIT DELAY
128
1 BIT DELAY
140
1 BIT DELAY
142
COMPLEX DIGITAL MATCHED FILTER
124
I
Q
132
134
136
138
α
148
Σ
146
+
−
149
THRESHOLD
DIFFERENTIAL DECODE
172
DATA OUTPUT
160
162
164
166
NORMALISE AMPLITUDE & THRESHOLD TO NEAREST PHASE IN ALPHABET
170
COMPLEX CONJUGATE
168

Fig.5

5/6

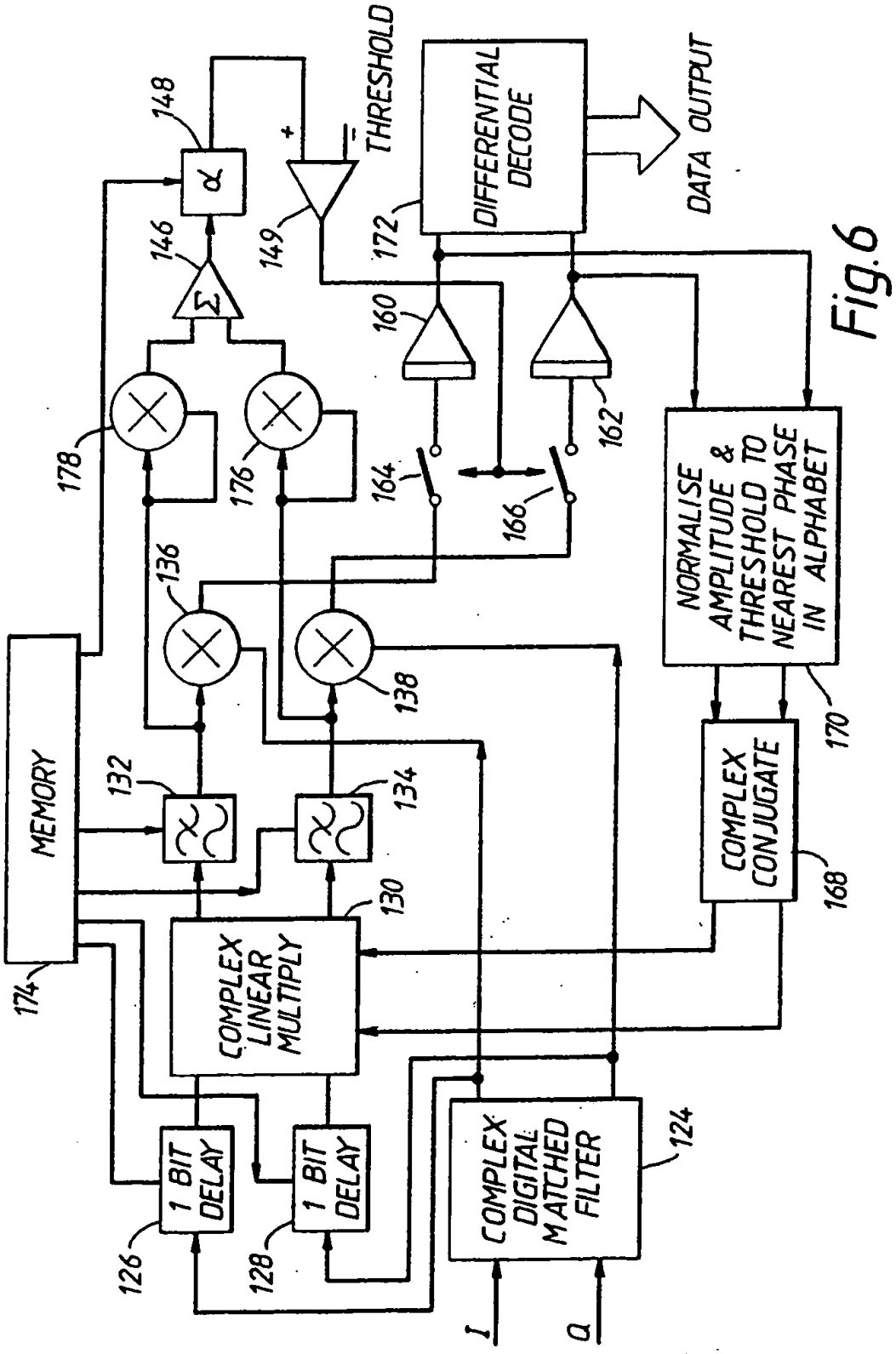
THRESHOLD
DIFFERENTIAL DECODE
DATA OUTPUT
148
146
149
172
160
162
178
176
164
166
136
138
NORMALISE AMPLITUDE & THRESHOLD TO NEAREST PHASE IN ALPHABET
170
MEMORY
132
134
130
COMPLEX CONJUGATE
168
174
COMPLEX LINEAR MULTIPLY
1 BIT DELAY
1 BIT DELAY
126
128
COMPLEX DIGITAL MATCHED FILTER
124
I
Q

Fig.6

# INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/GB 94/00585

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | ELECTRONICS LETTERS.,<br>vol.29, no.5, 4 March 1993, LONDON GB<br>pages 456 - 458, XP349861<br>R.S. MOWBRAY/P.M. GRANT/R.D. PRINGLE: 'New Antimultipath Technique for Spread Spectrum Receivers.'<br>see abstract<br>see page 456, right column, paragraph 1<br>see page 457, right column, paragraph 3; figures | 1-20 |
| A | Vehicular Technology Society 42nd VTS Conference, Denver, US, 10.-13.05.1992,<br>vol. 2, pages 1038-1041,<br>IEEE, New York, US; XP339957;<br>H. KAUFMANN/R. KÜNG/U. FAWER: 'Digital Spread-Spectrum Multipath-Diversity Receiver for Indoor Communications.'<br>see page 1038, right column, line 2 - page 1039, left column, paragraph 1; figures 1,2<br>see page 1041, right column, paragraph 1 | 1-20 |
| A | MILCOM 90. 1990 IEEE Military Communications Conference, Monterey, US,<br>30.09.-03.10.1990,<br>vol. 3, pages 1025-1029;<br>IEEE, New York, US; XP222000;<br>R.E. KANE JR./K.S. GONG/R.R. KURTH: 'Performance of a RAKE Demodulator with Pre-decision Multipath Thresholding.'<br>see page 1025, left column, paragraph 1 - page 1026, right column, paragraph 2; figures 1-3 | 1-20 |